

538,377

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property
Organization
International Bureau



(43) International Publication Date
24 June 2004 (24.06.2004)

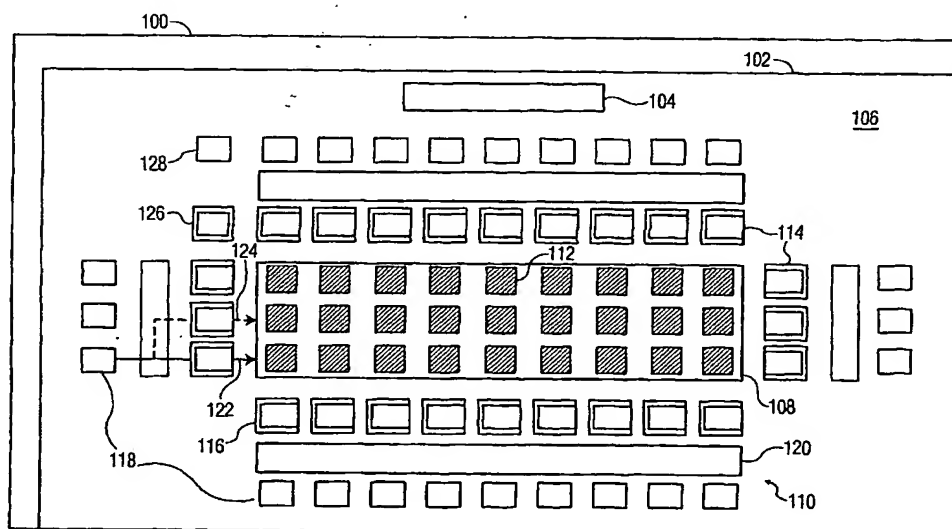
PCT

(10) International Publication Number
WO 2004/053716 A2

- (51) International Patent Classification⁷: **G06F 15/80**
- (21) International Application Number:
PCT/IB2003/005623
- (22) International Filing Date:
28 November 2003 (28.11.2003)
- (25) Filing Language: English
- (26) Publication Language: English
- (30) Priority Data:
60/432,971 12 December 2002 (12.12.2002) US
60/475,166 2 June 2003 (02.06.2003) US
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- (81) Designated States (*national*): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.
- (84) Designated States (*regional*): ARIPO patent (BW, GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).
- Declaration under Rule 4.17:**
— as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii)) for all designations
- Published:**
— without international search report and to be republished upon receipt of that report

[Continued on next page]

(54) Title: DATAFLOW-SYNCHRONIZED EMBEDDED FIELD PROGRAMMABLE PROCESSOR ARRAY



(57) Abstract: An embedded field programmable processor includes a two-dimensional array of processing cells for performing mathematical operations whose timing depends on the inflow of operands. An array interface reconfigurably connects paths for the inflow to respective cells on the array periphery. The array is preferably of the systolic type and is preferably implemented with nearest neighbor inter-cell connections.

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